Claim 16. (Previously Amended) The multilayer ceramic substrate of claim 13, wherein a shield pattern is provided at an outer edge of said conductive pattern.

Claim 17. (Previously Amended) The multilayer ceramic substrate of claim 13, wherein said ceramic substrate is provided with a through hole filled with an electroconductive substance and burned, and said via is disposed on the through hole.

Claim 18. (Previously Amended) The multilayer ceramic substrate of claim 13, further comprising a dielectric layer formed on a part of said ceramic substrate.

Claim 19. (Previously Amended) The multilayer ceramic substrate of claim 13, further comprising an LSI chip mounted on a part of one of said first and second conductive patterns with the face down and electrically connected.

Claim 20. (Previously Amended) The multilayer ceramic substrate of claim 13, further comprising an LSI chip mounted on a part of one of said first and second conductive patterns with the face down and electrically connected through an electroconductive paste applied on the top of a fine bump provided on one of said first and second conductive patterns, said fine bump formed by using a second groove which is disposed on said intaglio at a place corresponding to a pad of said LSI chip.

Claim 21. (Previously Amended) The multilayer ceramic substrate of claim 13, further comprising an LSI package mounted on a part of one of said first and second conductive patterns with the face down and electrically connected through a lattice of lands with a pitch of not larger than 0.8mm, said lattice provided on one of said first and second conductive patterns.

Claim 22. (Previously Added) The multilayer ceramic substrate of claim 14, wherein a meshed pattern is provided in a part of said conductive pattern.

Claim 23. (Previously Added) The multilayer ceramic substrate of claim 14, wherein a shield pattern is provided at an outer edge of said conductive pattern.

Claim 24. (Previously Added) The multilayer ceramic substrate of claim 14, wherein said ceramic substrate is provided with a through hole filled with an

electroconductive substance and burned, and said via is disposed on the through hole.

Claim 25. (Previously Added) The multilayer ceramic substrate of claim 14, further comprising a dielectric layer formed on a part of said ceramic substrate.

Claim 26. (Newly Added) The multilayer ceramic substrate of claim 14, further comprising an LSI chip mounted on a part of one of said first and second conductive patterns with the face down and electrically connected.

Claim 27. (Previously Added) The multilayer ceramic substrate of claim 14, further comprising an LSI chip mounted on a part of one of said first and second conductive patterns with the face down and electrically connected through an electroconductive paste applied on the top of a fine bump provided on one of said first and second conductive patterns, said fine bump formed by using a second groove which is disposed on said intaglio at a place corresponding to a pad of said LSI chip.

Claim 28. (Previously Added) The multilayer ceramic substrate of claim 14, further comprising an LSI package mounted on a part of one of said first and second conductive patterns with the face down and electrically connected through a lattice of lands with a pitch of not larger than 0.8mm, said lattice provided on one of said first and second conductive patterns.